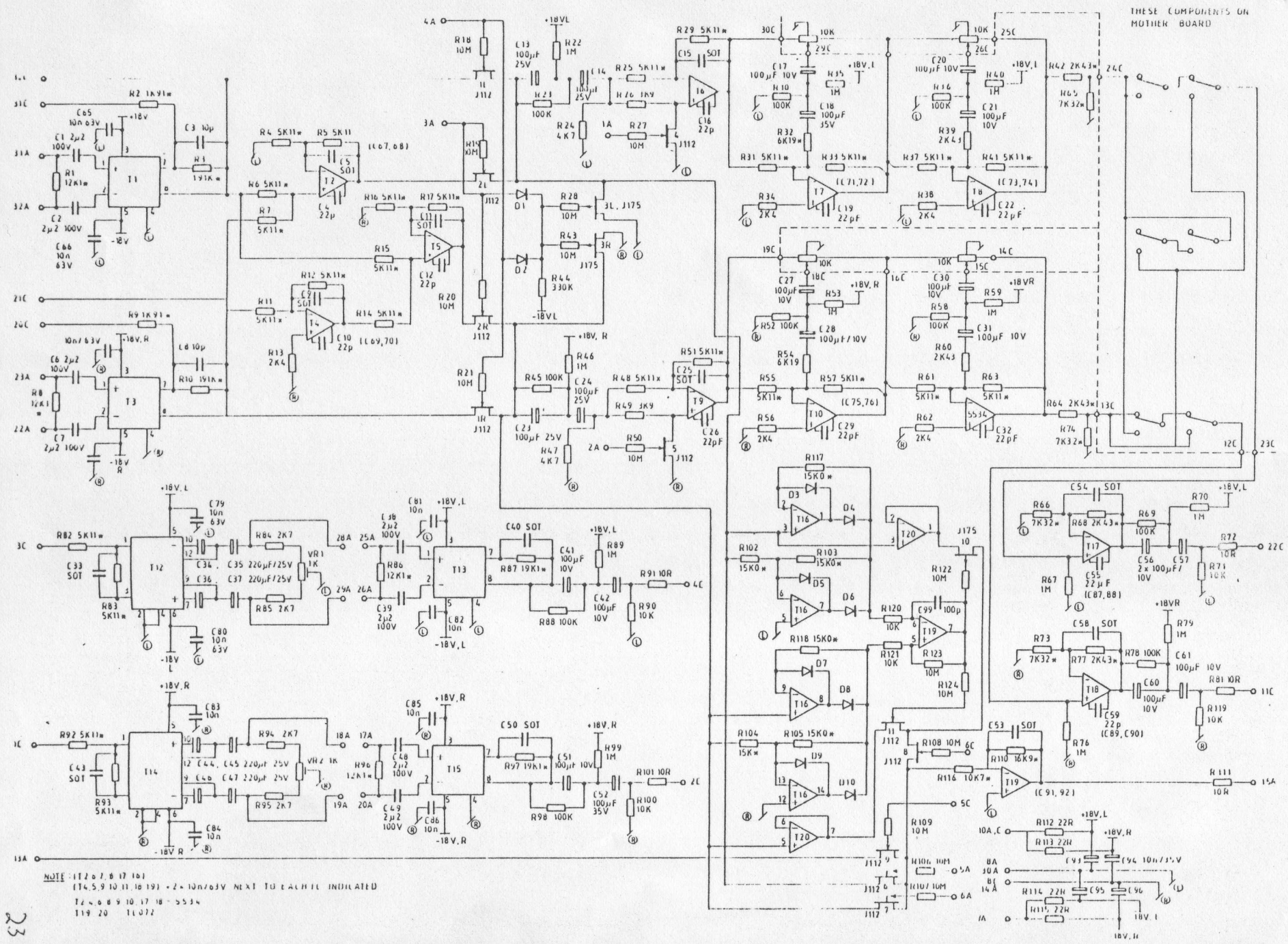




Copyright © SSL All rights reserved.
This document may not be
reproduced in any form without the
written permission of SSL

T82201-70 STEREO LINE
INPUTS INSERTS SENDS &
RETURNS

Orig No. T82201-70

Solid State Logic

MF 103018

64 Way DIN 41612 Connector List

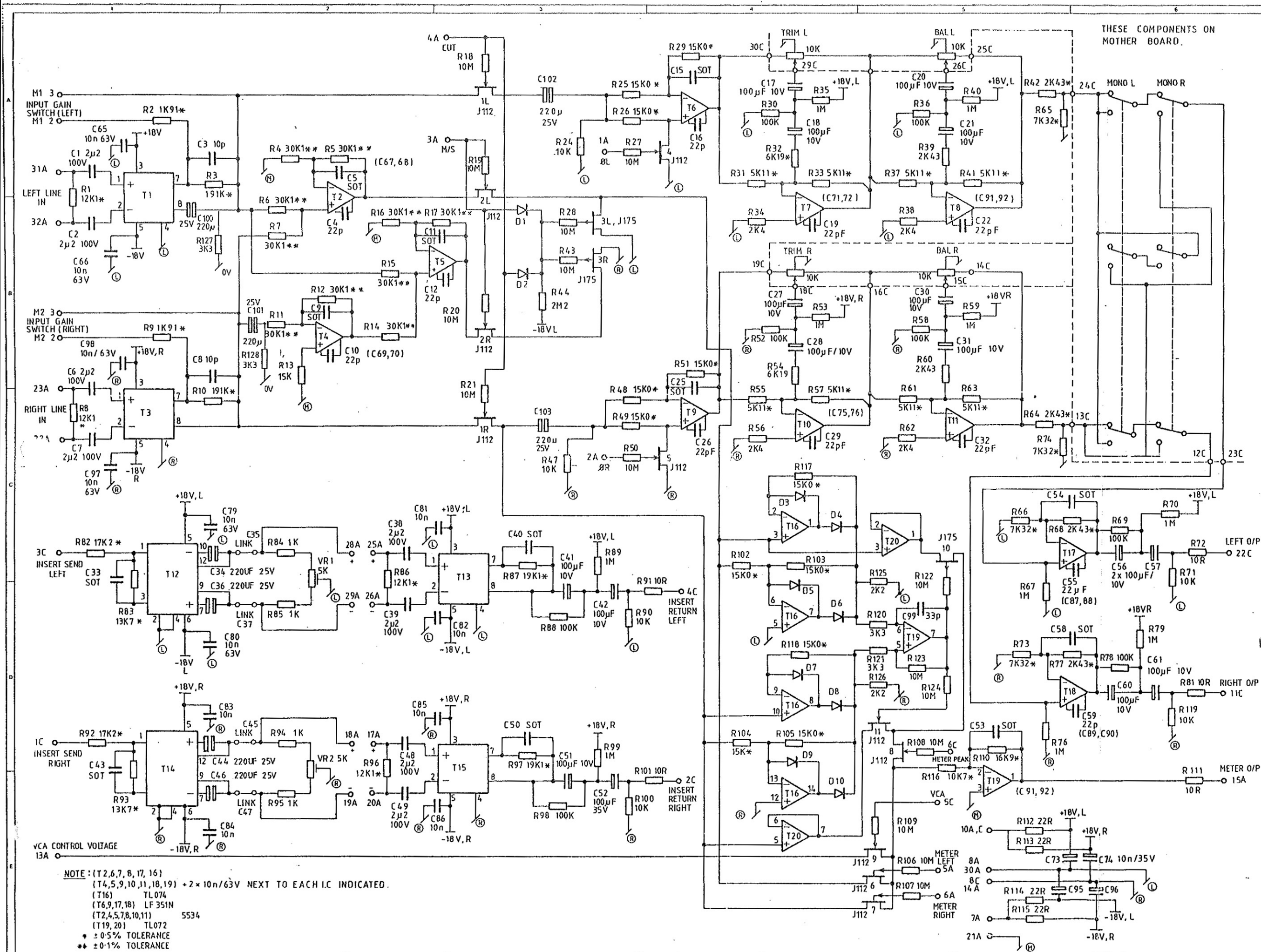
From: 611S Mother board

To: 82E201 Stereo line inputs, insert sends & returns.

No	Row A	No	Row C
1	0L FET	1	Insert R send from Switchcard
2	0R FET	2	Insert R return to Switchcard
3	M/S FET	3	Insert L send from switchcard
4	A/B FET	4	Insert L return to Switchcard
5	Meter L FET	5	VCA to meter FET
6	Meter R FET	6	Meter peak FET
7	-18V	7	-18V
8	0V (L)	8	0V (R)
9	Not Used	9	Not Used
10	+18V	10	+18V
11	Not used(+48V in)	11	R output
12	Not used(+48V out)	12	R output buffer input
13	VCA control voltage	13	Mono R Switch send
14	0V (R)	14	R Balance control ACW
15	Meter output	15	R Balance control Wpr
16	0V (R)	16	R Balance control CW / Trim ACW
17	Insert R return +	17	Spare -
18	Insert R send +	18	R Trim control Wpr
19	Insert R send -	19	R Trim control CW
20	Insert R return -	20	Gain switch R
21	0V (M)	21	Gain switch R wiper
22	Line in R -	22	L output
23	Line in R +	23	L output buffer input
24	0V (L)	24	Mono L switch send
25	Insert return L +	25	L Balance control CW
26	Insert return L -	26	L Balance control Wpr
27	Insert L send from Switchcard	27	L Balance control ACW / Trim ACW
28	Insert send L +	28	Spare
29	Insert send L -	29	L Trim control Wpr
30	0V (L)	30	L Trim control CW
31	Line in L +	31	Gain switch L
32	Line in L -	32	Gain switch L wiper

T82201.50

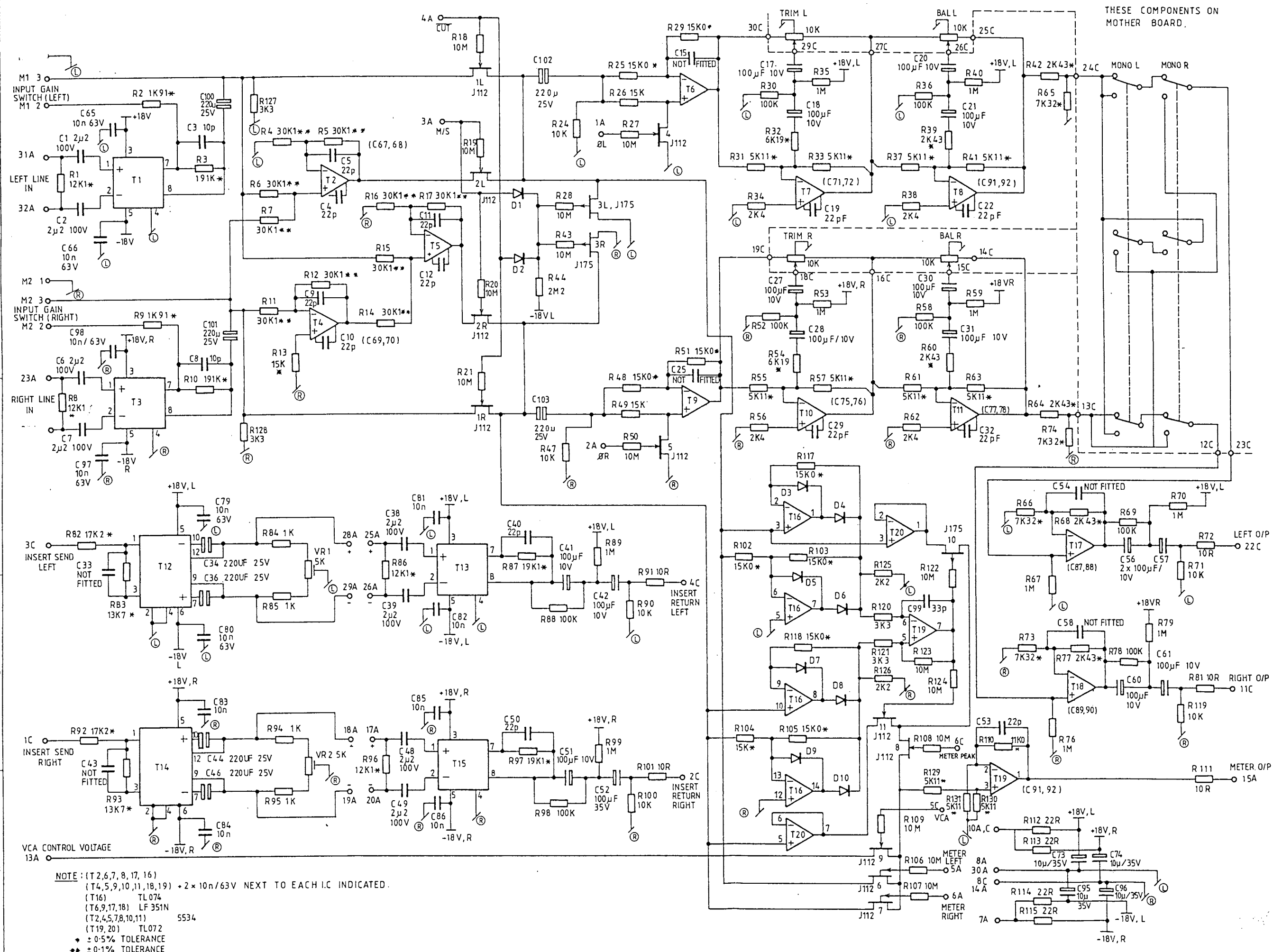
29 Aug 84



Copyright © SSL All rights reserved. This document may not be reproduced in any form without the written permission of SSL.			
Rev.	Issue	Chkd	Details
P	a	7-84	PROTOTYPE
1	a	7-84	R65 74 MOVED & CHANGED VALUE R67 R76 TO 1M
2	a	7-84	R117, 118 ADDED
2	b	7-84	METER PEAK CIRCUITRY CHANGED
2	c	1-85	MS AND 0 VALUES CHANGED
2	d	7-84	REDRAWN O.D.
3	a	4-85	R120, 121 CHANGED 2x2K2's ADDED
3	b	4-85	R44 NOW 2M2
4	a	7-85	R84, 85, 94, 95 VALUE NOW 1K. VR1, VR2 VALUE NOW 5K
4	b	Apr 86	BC EON ADDRESSES ADDED NOTE AMENDED
4	c	June 86	MONO L & MONO R REVERSED
5	a	Dec 86	R22, 23, 45 & 46: C13, 14 23 & 24 DELETED: R128 3K3 + R127 3K3 & C100, 101, 102 + 103 220p ADDED
6	a	May 87	T17 & 18 IC LIN AMP NOW IC LIN BIFET APP REF. L7351N
7	a	May 87	R82, 83, 92 & 93 WERE 5K11. C34-7 & C44-7 WERE CAP ELECT. 220UF 25V.
Title 82E201 STEREO LINE INPUTS INSERTS SENDS & RETURNS			
Drg. No. T82201-70			
Solid State Logic			

64 Way DIN 41612 Connector List	
From: 611S Mother board	
To: 82E201 Stereo line inputs, insert sends & returns.	
No Row A	No Row C
1 0L FET	1 Insert R send from Switchcard
2 0R FET	2 Insert R return to Switchcard
3 M/S FET	3 Insert L send from switchcard
4 A/B FET	4 Insert L return to Switchcard
5 Meter L FET	5 VCA to meter FET
6 Meter R FET	6 Meter peak FET
7 -18V	7 -18V
8 0V (L)	8 0V (R)
9 Not Used	9 Not Used
10 +18V	10 +18V
11 Not used(+48V in)	11 R output
12 Not used(+48V out)	12 R output buffer input
13 VCA control voltage	13 Mono R Switch send
14 0V (R)	14 R Balance control ACW
15 Meter output	15 R Balance control Wpr
16 0V (R)	16 R Balance control CW / Trim ACW
17 Insert R return +	17 Spare -
18 Insert R send +	18 R Trim control Wpr
19 Insert R send -	19 R Trim control CW
20 Insert R return -	20 Gain switch R
21 0V (M)	21 Gain switch R wiper
22 Line in R -	22 L output
23 Line in R +	23 L output buffer input
24 0V (L)	24 Mono L switch send
25 Insert return L +	25 L Balance control CW
26 Insert return L -	26 L Balance control Wpr
27 Insert L send from Switchcard	27 L Balance control ACW / Trim ACW
28 Insert send L +	28 Spare
29 Insert send L -	29 L Trim control Wpr
30 0V (L)	30 L Trim control CW
31 Line in L +	31 Gain switch L
32 Line in L -	32 Gain switch L wiper

T82201.50
29 Aug 84



Copyright © SSL All rights reserved.
 This document may not be
 reproduced in any form without the
 written permission of SSL

Rev	Issue	Chkd	Details
P	a	7-84	PROTOTYPE
1	a	7-84	R65 74 MOVED & CHANGED VALUE R67 R76 TO 1M
2	a	7-84	R117, 118 ADDED
2	b	7-84	METER PEAK CIRCUITRY CHANGED
2	c	1-85	MS AND 0 VALUES CHANGED
2	d	7-84	REDRAWN O.D.
3	a	4-85	R120, 121 CHANGED 2x2K2's ADDED
3	b	4-85	R44 NOW 2M2
4	a	7-85	R84, 85, 94, 95 VALUE NOW 1K. VR1, VR2 VALUE NOW 5K
4	b	BC Apr 86	ECON ADDRESSES ADDED NOTE AMENDED
4	c	DTIC June 86	MONO L & MONO R REVERSED
5	a	Dec 86	R22, 23, 45 & 46: C1314 23 & 24 DELETED - R128 3K3 + R127 3K3 & C100, 101, 102 + 103 220 μ ADDED
6	a	May 87	T17 & 18 IC LIN AMP NOW IC LIN BIFET AMP REF: LF351N
7	a	DM May 87	R82, 83, 92 & 93 WERE 5K11. C34-7 & C44-7 WERE CAP ELECT. 220UF 25V.
7	b	Nov 87	LINK ADDED ADJ. C102 & ADJ. C103.
7	c	12 JULY 89	C16: 26: 55: 59 DELETED. LINKS C35: 37: 45: 47 TH DELETED. C5: 11: 33: 40: 43 50: 53 VALUES ADDED
8	a	12 JULY 89	ECO 4K/409 R116 DELETED. R110 WAS 16K9 NOW 11K0. R129-131 5K11 ADDED. STEFF
8	b	24 OCT 89	* ADDED TO R13: 39: 54: 60. STEFF
9	a	21 MAR 90	ECO 4K/492 INTRODUCTION OF L/N PCB
10	a	SEPT 90	ECO 4K/622 B.O.M. AMENDED STEFF

SHEET 1 OF 1

Title 82E201 STEREO LINE
 INPUTS INSERTS SENDS &
 RETURNS

Org. No. T82201-70

Solid State Logic

2-7